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This report describes results of a project on optical interconnects for multichip modules performed by UNC-Charlotte and MCNC. The basic concept was to attach edge-emmitting laser array chips, micro-mirror chips, photodetectors and computer-generated holograms to a glass substrate. With the aid of these components, signals can be routed between chips on a MCM by optical means rather than electrical means.

Work was achieved in four areas: laser arrays, photodetectors, computer generated holograms and system integration.

This work enabled the demonstration of what we believe to be the first complete optical link between chips on a multichip module without active alignment. This is important because active alignment is not practical for production of such systems.

This work was achieved from breakthroughs in 3 areas. First a novel scheme for designing the computer generated holograms enabled the links to be performed with very high light efficiency. Second the method of integration and packaging enabled highly accurate placement of the components using flip-chip technology. Third, a novel method for fabricating detectors and integrating them with integrated circuits, greatly reduced the power dissipation of the links.

(Abstract)

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1. Introduction

For the past few years we have been working on the development of an optically interconnected Multichip Module (MCM) [1-4]. A schematic diagram illustrating the basic approach used in our first prototype system is shown in Fig. 1. The MCM is composed of a planar transparent substrate, containing thin film electrical connections. GaAs laser array chips and silicon CMOS VLSI chips with integrated photodectors are flip-chip bonded to one side of the substrate, while Computer Generated Holograms (CGHs) are fabricated on the other side of the substrate.

The purpose of this work is to develop the technology to enable high speed and high density connections between chips, MCMs and PC boards. We believe that the basic approach shown in Fig. 1 and based on flip-chip and CGH technology will provide 1-2 orders of magnitude increase in connection performance when compared with conventional electrical connectors.
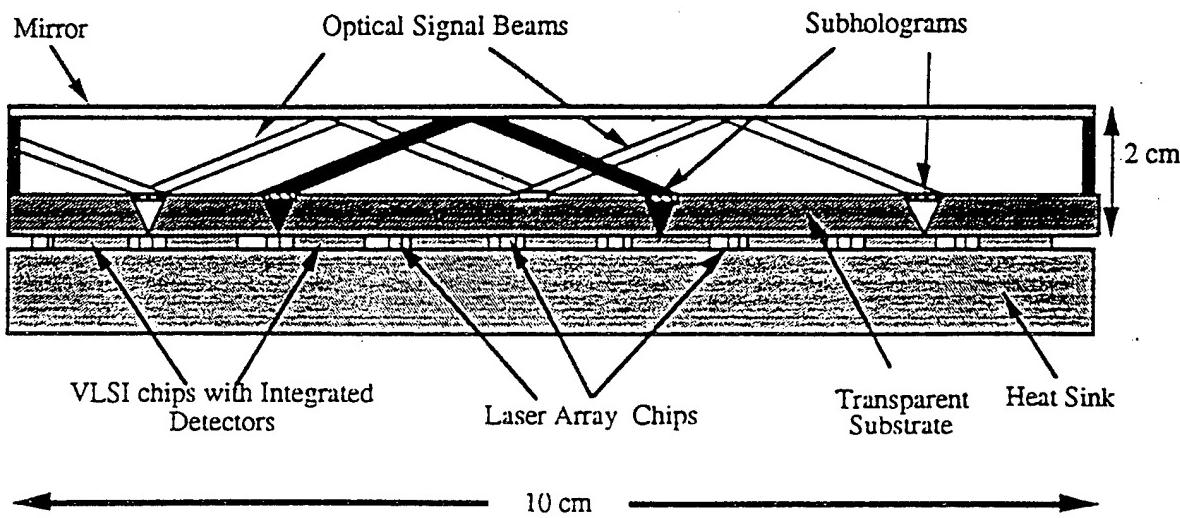

Figure 1. Cross sectional view of Optical Interconnected Multi-Chip Module (OIMCM).

In order to demonstrate this technology, we are building two prototype systems. The first prototype, illustrated schematically in Fig. 1 and described in Refs. [2-4] , contains 85 optical links, 3 GaAs laser array chips and 12 silicon CMOS detector chips. Each laser array chip contains 32 edge-emitting lasers. The output of the edge-emitting lasers are redirected with the use of a gold coated silicon micro mirror. Each link was designed to operate at ~200 Mbit/sec.

In this paper we present experimental results of this first prototype system, referred to as the System 1 prototype. We believe this to be the first experimental demonstration of a complete free-space optical interconnect for a MCM.

This demonstration builds off of foundations provided by a large number of previous efforts in this area. For example in Ref. [1], experimental free-space interconnect links were demonstrated between a discrete laser device and a VLSI chip using a CGH. However, neither chip was integrated to an MCM or PC board. Both were aligned with manual translation stages. In Ref. [5] a 1 Gbit/sec free-space link was demonstrated between a laser and a detector. Each was placed on an individual PCB but again both were aligned with manual translation stages. In Ref. [6], researches at Bell Labs demonstrated optical links between several GaAs chips that contained integrated modulators. However, the chips were again not integrated onto MCMs or PC boards but instead each chip was mounted on an individual translation stage.

The use of manual translation stages to align the chips in previous demonstration systems has brought criticism and skepticism from many in the electronics community. Many researchers have stated that the major disadvantage of free-space optical interconnects is the difficulty of alignment.

In Ref. [2], the use of CGHs combined with flip-chip technology to solve this alignment problem was first proposed. Successful flip-chip bonding of a laser diode for optical interconnects was first reported in Ref. [7]. This system also used CGH technology, but used thermal compression flip-chip bonding, rather than the self-aligning C4 process used for our prototype.

The remainder of this paper is organized as follows. In section 2, the optoelectronic devices are described. In section 3 and 4 the CGH technology and flip-chip technology employed is related. The experimental optical link results are presented in section 5.

2. Optoelectronic Devices

2.1. Laser Arrays
The optical signal transmitters employed in our system 1 prototype are edge-emitting lasers. The output of these edge-emitters are redirected with the use of a micro-mirror.

The edge-emitting laser array chips were described in Refs. [4, 8]. Each contains 32 laser elements, spaced

on a 250 micron pitch. The dimensions of each chip is 300 μm x 300 μm by 1 cm. A photograph of a single laser array chip is shown in Fig. 2. The laser array chips were experimentally measured to have operating speeds in excess of 500 Mbps. The threshold currents of the lasers were measured to be between 8 and 15 mA.
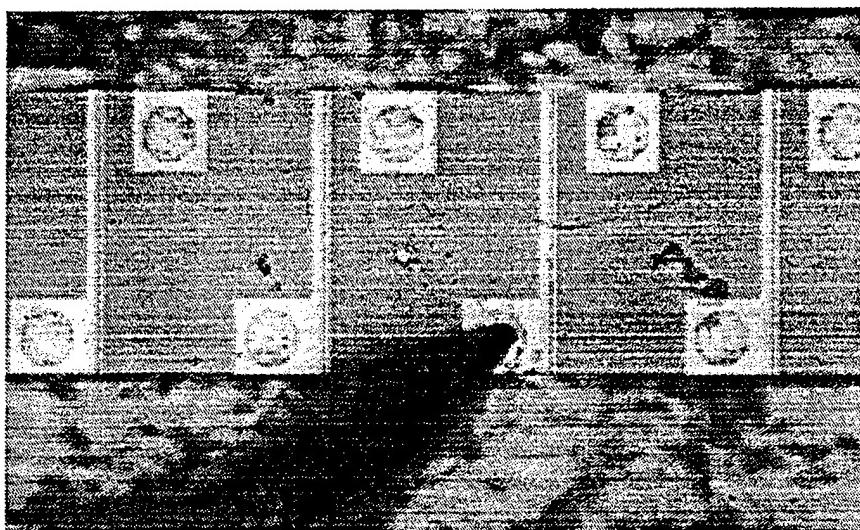

Figure 2. GaAs laser array chip showing flip-chip bonding pads and electrical probe making contact to one bonding pad [4, 8].

2.2. Photodetectors

As shown in Fig. 1, the photodetectors in our system 1 prototype were integrated directly onto a CMOS VLSI chip. There are several advantages to this approach in comparison to more conventional approaches employing discrete silicon or GaAs detectors. First, CMOS is less expensive and generally dissipates less power than GaAs and bipolar silicon. Second, integration of the detector avoids the power dissipation and time delay needed to drive the bonding pads required with the discrete detector approach to send a signal to the VLSI chip. This is especially significant when fanout of the signal is needed.

The major disadvantage of using integrated CMOS photodetectors is their limited operating bandwidth. In Ref. [9] an integrated photodetector fabricated with a MOSIS 3 micron CMOS process was reported. Its maximum datarate was reported to be limited to ~5 Mbits/sec. However, as described in Ref. [10], we developed an improved CMOS photodetector by modifying MCNC's standard 1.25 μm CMOS process. The process was modified by incorporating a deep intrinsic well for location of the photodetectors. These detectors were measured to operate at 220 Mbits/sec. Simulation results indicate that by further modifications of the process and small modifications to the circuit design, datarates of 500 Mbits/sec to 1 Gbit/sec are feasible.

3. Computer Generated Holograms

diffraction efficiency under 3 conditions for which they typically have low efficiency: (1) low F#'s, (2) large deflection angles and (3) operation over a large bandwidth (~10-20 nm).

3.1. Low F#'s

Typical full width divergence angles of semiconductor lasers are ~25 x 50 degrees. This corresponds to a CGH F# requirement of at least F/2.3 by F/1.1. Microlenses with such low F#'s made with CGH technology typically have very low diffraction efficiency. For example in Ref. [11] it is shown that for an F/1 lens with a wavelength of 0.8 μm, the grating period at the edge of the lens is 1.8 μm. If a 0.7 μm minimum feature size is employed, only 2 phase levels can be employed, reducing the maximum diffraction efficiency with traditional CGH encoding methods (i.e. the Analytic Quantization (AQ) method[11]), to 40%.

In order to increase the diffraction efficiency of CGH's with low F#'s a new design/encoding method was developed at UNC-Charlotte. This method is termed Radially Symmetric Iterative Discrete On-axis (RSIDO) encoding. In Ref. [11], it was shown that this method can be used to increase the diffraction efficiency of an F/1 element to > ~90%.

3.2. Large Deflection angles

In order to reduce the overall volume of the MCM, it is important for the CGH to be able to deflect an optical link at a large angle (e.g., 15-35 degrees with respect to the normal).

In Ref. [7], CGH technology was used to demonstrate an optical link with a deflection angle of 9.5 degrees. It is also explained in this reference that for such a large deflection angle, only 2 phase levels can be employed due to the small grating period required, limiting the maximum diffraction efficiency of each CGH to 40%. Since 2 CGH's are typically required per link (see Ref. 12), this limits the maximum optical link efficiency to 16%.

In order to improve the diffraction efficiency of CGH's for large deflection angles, we developed a modified version of the RSIDO encoding method, termed Segmented Radial Partitions (SRP). With the SRP method the CGH is divided into arc-shaped radial segments. Within each segment the RSIDO method is employed, where radial symmetry is required. However, over the entire CGH element, non-radially symmetric patterns can be generated. With this method, simulation results indicate that diffraction efficiencies of 80% can be achieved for angles as large as 27 degrees.

3.3. Large Optical Bandwidth

The large optical bandwidth requirements are due primarily to 2 sources: (1) wavelength variance of the lasers with thermal fluctuations and (2) variance of center wavelength of the laser at room temperature among GaAs chips.

The typical wavelength dependence of semiconductor lasers on temperatures is ~0.33 to 0.4 nm/degree °C.

Thus a thermal variance of $\pm 10\,°C$ corresponds to a center wavelength variance of ± 3 nm. In addition, due to variances in the nominal center wavelength of each laser between different GaAs chips, an optical bandwidth of ~10-20 nm is required.

In Refs. [11, 13] it is shown that the RSIDO method can also be used to minimize a CGH's sensitivity to wavelength variations. For example in Ref. [13], an F/1 element was designed and fabricated for operation over a ± 12.5 nm optical bandwidth. While the spot produced by this element at the center wavelength is slightly larger than diffraction limited, the spotsize near the edge of the optical bandwidth is a factor of 3 times smaller than an analytically designed element.

3.4. CGH's for prototype

As stated in Section 1, the System 1 prototype contains 3 laser array chips, each containing 32 laser elements, spaced on a grid with a 250 micron period. However, in order to minimize crosstalk and optimize connection density a CGH diameter of 500 microns was chosen, so that only 16 of the 32 lasers per chip are employed for an optical link in the System 1 prototype. This allows for 16 independent optical channels per chip. Each channel has fanout ranging from 1-3 resulting in ~30 optical links per chip and ~90 optical links in total.

In order to fabricate the CGH's for such a large number of interconnects, it is important to employ a Computer Aided Design (CAD) system. In this regard we have developed a limited optical interconnect CAD system by writing routines to supplement the commercial CAD tool made by Cadence™ and routines to interface to our in-house CGH encoding software. All connections can then be laid out in a single file. A photograph of all the connections for the system 1 prototype in our CAD system is shown in Fig. 3. Note that the system consists of 3 rows. Each row is identical consisting of one laser array chip and 4 silicon CMOS chips.

The particular optical connections were chosen to demonstrate a range of connection angles, connection lengths and fanouts. In addition, connections made through multiple reflections between the mirror and CGH substrate (as shown in Fig. 1) were also implemented.

4. Flip-chip Attachment for System Integration & Packaging

As mentioned in Section 1, one of the main criticisms of free-space optical interconnects in the past has been the difficulty in achieving the required alignment tolerances. In order to solve this problem we have developed a packaging scheme that is based on the use of CGHs in a double pass configuration [12] as well as the use of self-aligning flip-chip technology.

Alignment of the mirror in Fig. 1 to the chip and alignment between holograms is relatively non-critical

Since the size of each of the hologram facets is ~500-750 microns, a misalignment of the beam position on a detector subhologram by 1-2 mils will not significantly affect the CGH performance.

The most critical alignment requirement is that of each CGH facet to the detector or laser located directly beneath it. Since the size of each detector varies between 15 to 25 micron, the tolerance on this alignment is ~2 to 5 microns, depending the particular detector size employed. This alignment is achieved as follows. First the CGH's are photolithographically defined on the top side of the substrate. Next a metal alignment layer is photolithographically placed on the bottom side of the substrate using a through-wafer mask aligner to align the level to the layers on the top side. The underbump metallurgy for the solder bumps are then photolithographically defined by aligning with respect to the metal alignment layer.

The alignment accuracy of each layer to another layer on the same side is less than 0.5 μm with a conventional contact mask aligner. However, the through wafer alignment step has an accuracy of ~1-5 microns, depending on the precise method employed and the thickness of the substrate.

The micro-mirrors for redirection of the output of the edge emitting lasers were also attached to the substrate with flip-chip bonding techniques. The micro-mirrors were formed by photolithographically defining mirror well regions with respect to the flip-chip bump locations on a silicon chips. The well locations were then chemically etched along a crystalline plane to form the mirror at a precise angle. A photograph of a cross-section of an MCM showing a laser and mirror attached to an MCM with flip-chip solder bumps is shown in Fig. 4.
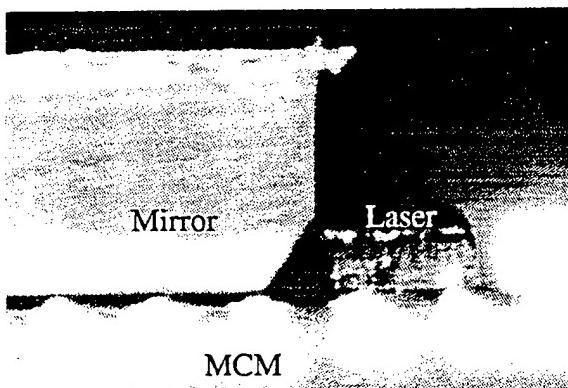

Figure 4. Photograph of silicon mirror chip (left) and GaAs laser array chip (right) flipchip bonded to the MCM substrate (bottom).

5. Prototype Experimental Measurements

A photograph of the System 1 prototype containing the laser chips, silicon chips and integrated CGHs is shown in Fig. 5.

The optical output power emitted by each laser averaged ~1 mW per facet. (Light was emitted from both

sides of the laser, since no anti-reflection coatings were employed.) Of the 1 mW per facet only ~1/2 of this power was reflected by each gold coated silicon micro-mirror and redirected to a CGH facet located above each laser. Since the average efficiency of each CGH facet was ~ 75%, only approximately 200-300 μW of power was deflected by the CGH towards the appropriate location. Taking into account loses due to misalignment on the receiving subhologram, misalignment on the detector, diffractive losses on the second CGH facet and fresnel losses at the 2 air glass interfaces and 1 air-silicon interface, we estimate that only ~50 μW was available for detector activation.

Figure 5 shows a photograph of the MCM with a single laser activated, taken with a CCD camera. A spot over the laser indicating its emission is clearly evident. Light reflecting off of a receiving CGH facet is also visible. Note that the light emanating from the laser is much brighter, since it is directed toward the CCD camera while the light reflecting from the CGH is very dim, since only a small percentage of the light is reflected by the CGH facet. The intermediate spots were taken by overlapping multiple CCD frame grabs that were taken with the room lights out and a card placed at several locations along the beam propagation path.
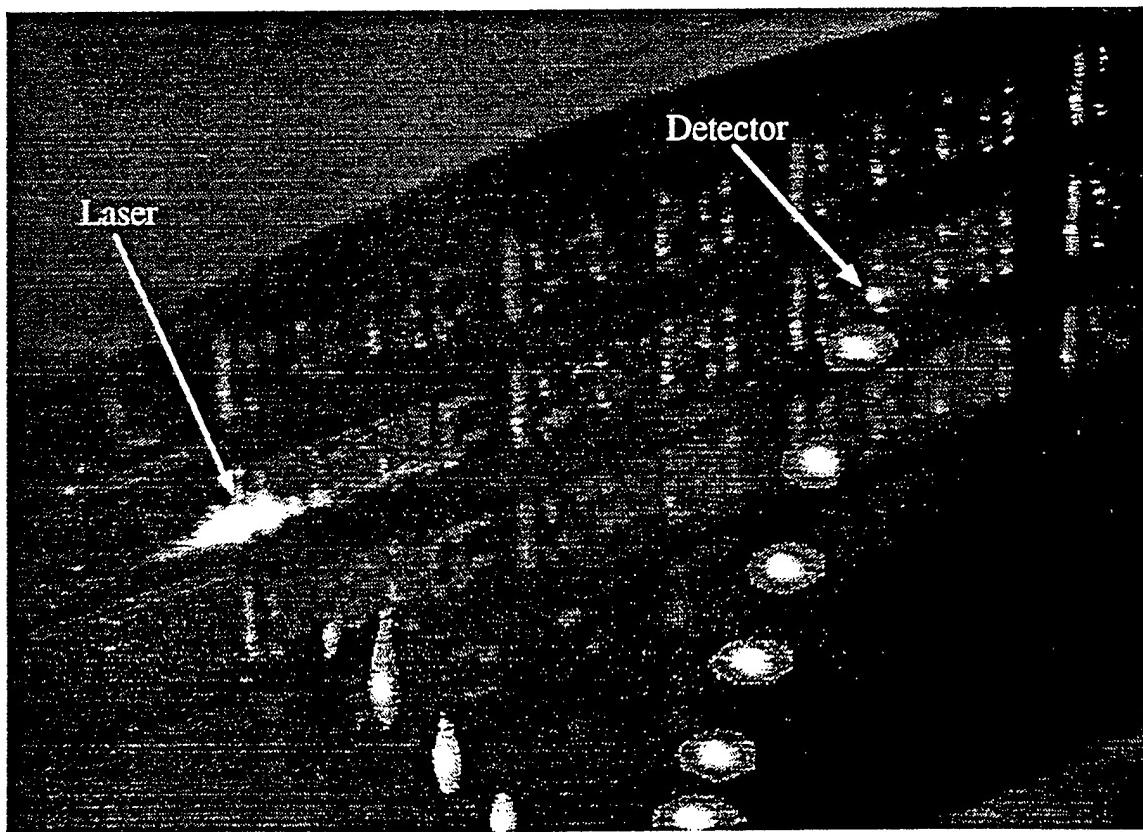

Figure 5. Image showing an optical link between one laser element and one detector on a silicon VLSI chip.

Figure 6 shows a scope trace of a signal transmitted by the optical interconnect. Fig. 6a shows an electrical signal that was input to a particular optical link. Note that the rise time of this signal was 18 nsec. Fig. 6b shows the fall time of the signal after transmission through the optical link and is equal to the voltage on an

MCM bonding pad driven by a detector amplifier gate. Due to the inverting properties of the detector receiving circuitry the output signal falls when the input signal rises. Note that the fall time on the output pad of 18 nsec, shows that the increase in rise/fall time due to the optical link is negligible for an 18 nsec signal.

6. Conclusions

This work presents what we believe to be the first experimental demonstration of a complete free-space optical interconnect between chips within a Multichip Module (MCM). All chips were flip-chip bonded to a single transparent substrate that also contained integrated Computer Generated Holograms (CGHs).

This demonstration was made possible due to technological advances made during the last few years in three different areas. First, high-speed photodetectors with high quantum efficiency that could be integrated within a CMOS VLSI chip were developed. These detectors, described in Ref. 10, enabled an order of magnitude increase in response speed for integrated CMOS detectors with reasonable quantum efficiency. Second, new CGH design methods were developed [4] enabling a much higher diffraction efficiencies to be achieved for holograms requiring large deflection angles. Finally flip-chip bonding and other advanced packaging techniques were adopted for use with optical interconnects in order to achieve the required alignment accuracies.

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Holographic Optical Interconnects for MCM's

## The University of North Carolina at Charlotte

ARPA

Objectives

- Interconnect Density of 10,000 lines/cm for both chip-to-chip and MCM-to-MCM Interconnects

- Density-Speed Product of 20 Tbps for both Interchip and InterMCM Interconnects

- Build Prototype System to Demostrate Optical Interconnect Potential Performance and Limitations

Approach

- Optical Interconnects
- Computer Generated Holograms
- Flip-Chip Bonding
- Integrate Detectors onto Silicon Chips
- GaAs Laser Arrays

Status/Accomplishments

- Developed New CGH encoding Method (SRP) to increase link efficiency for large deflection angles from 4% to 65%

- Fabricated silicon CMOS detector with a datarate of 220 Mbits/sec (fastest previously reported CMOS detector operated at <10 Mbits/sec)

- First demonstration of complete Free-Space Optical Interconnect Link
  - 62 Mbits/sec verified experimentally
  - Experimental link density of 1400 I/Os/sq. cm
  - Equivalent to 2.0 μm 2-level electrical wiring pitch on a 4 inch MCM substrate
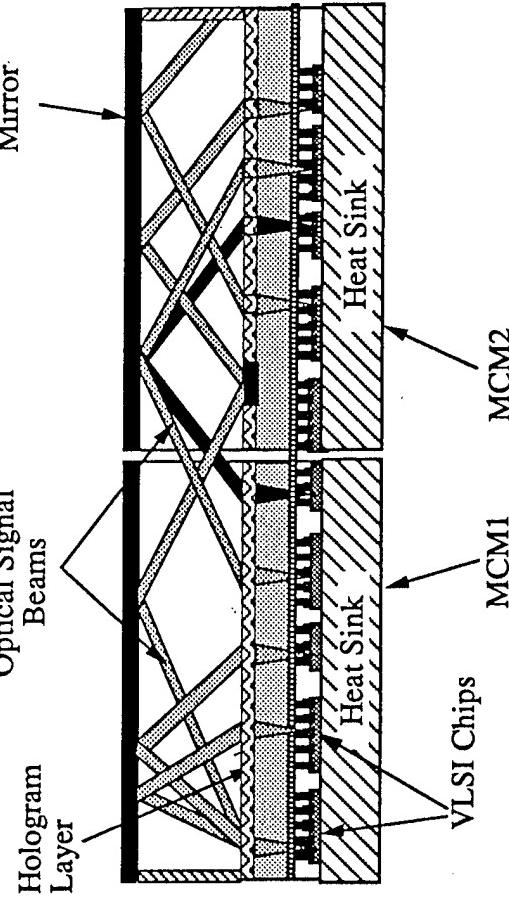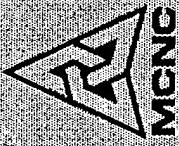
Mirror

Optical Signal Beams

Hologram Layer

VLSI Chips

Heat Sink

Heat Sink

MCM1   MCM2

Overview

First Experimental Demonstration of Complete Free-Space MCM Optical Link

Mirror

Optical Signal Beams

Subhologram

2 cm

Transparent Substrate

Heat Sink

Laser Array Chips

VLSI chips with integrated Detectors

10 cm

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MCNC
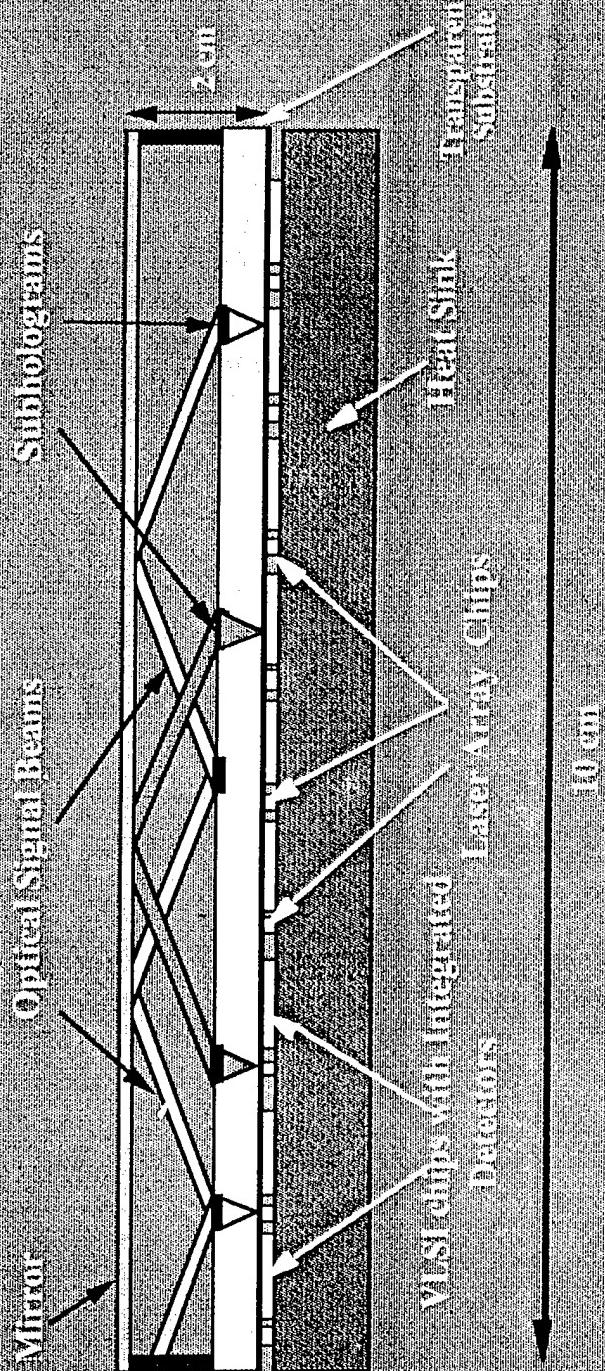
Tasks

- Photodetectors
- Lasers
- Holograms
- System Integration

System Specifications

System 1

85 Optical Links
200Mb/s Data Rate

System 2

1024 Optical Links
500Mb/s - 1Gb/s Optical Data Rate
100 - 200Mb/s VLSI Clock Speed

Laser Diode Arrays

Issues

- Individually Addressable Arrays Compatible with Flip-Chip Technology

- Low Threshold Currents

- Surface-emitting vs. Edge-emitting

Edge-Emitting
vs.
Surface-Emitting Lasers

Advantages of Edge-Emitters

- Cost, Availability (near term)
- Efficient Heat-sinking
- Known Reliability

Disadvantages of Edge-Emitters

- More Complex Packaging
- Cost, long term

Our Decision

- System 1: Edge-Emitters
- System 2: Surface-Emitters

Laser Array Chip

300μm

250μm

metal

8nm Qw
Al Ga As
0.05 0.95

1μm

SLs

p-AlGaAs 1.5μm (Al ~ 45%)

graded p-AlGaAs 0.2μm (Al ~ 45-20%)

graded n-AlGaAs 0.2μm (Al ~ 45-20%)

n-AlGaAs 1.5μm (Al ~ 45%)

n-GaAs Substrate
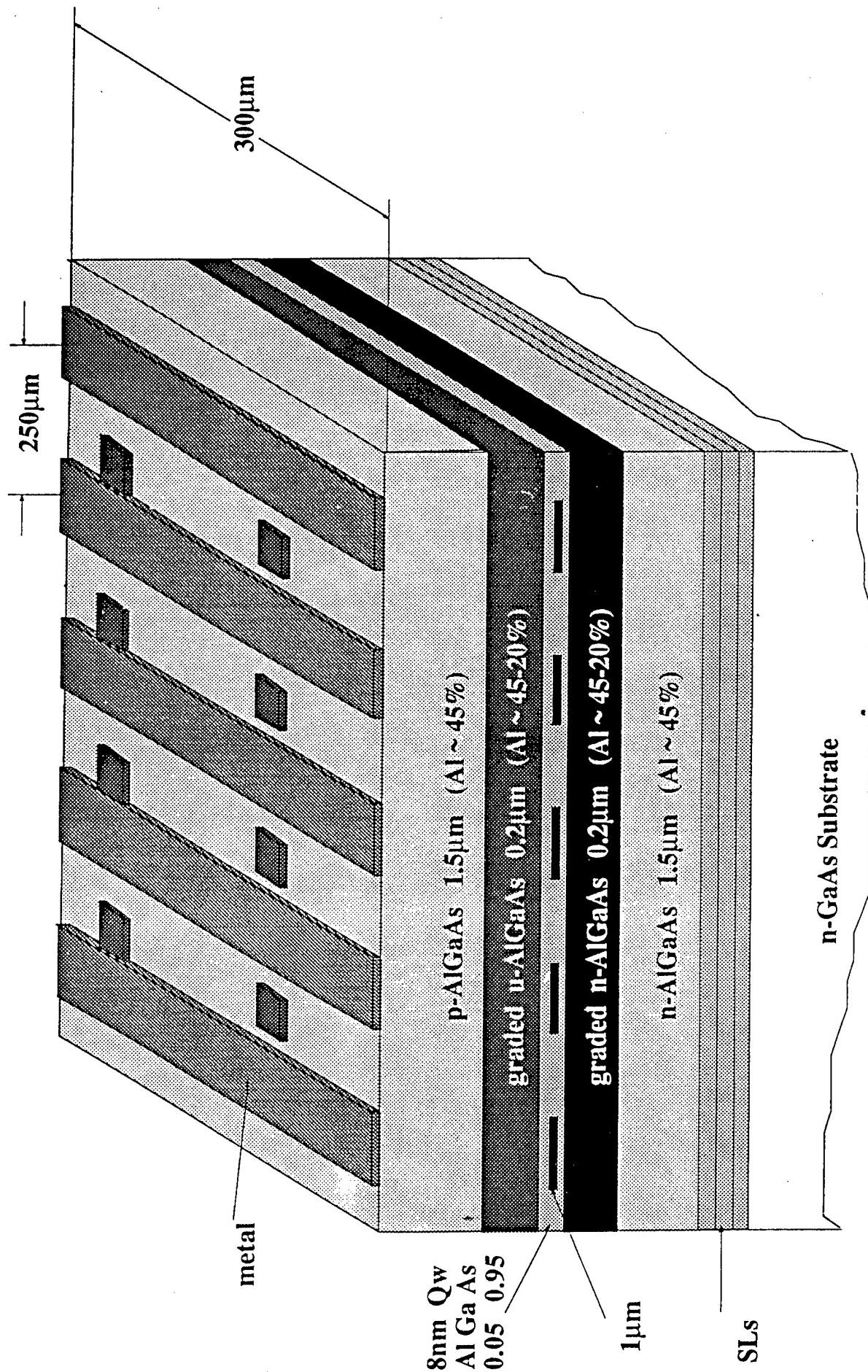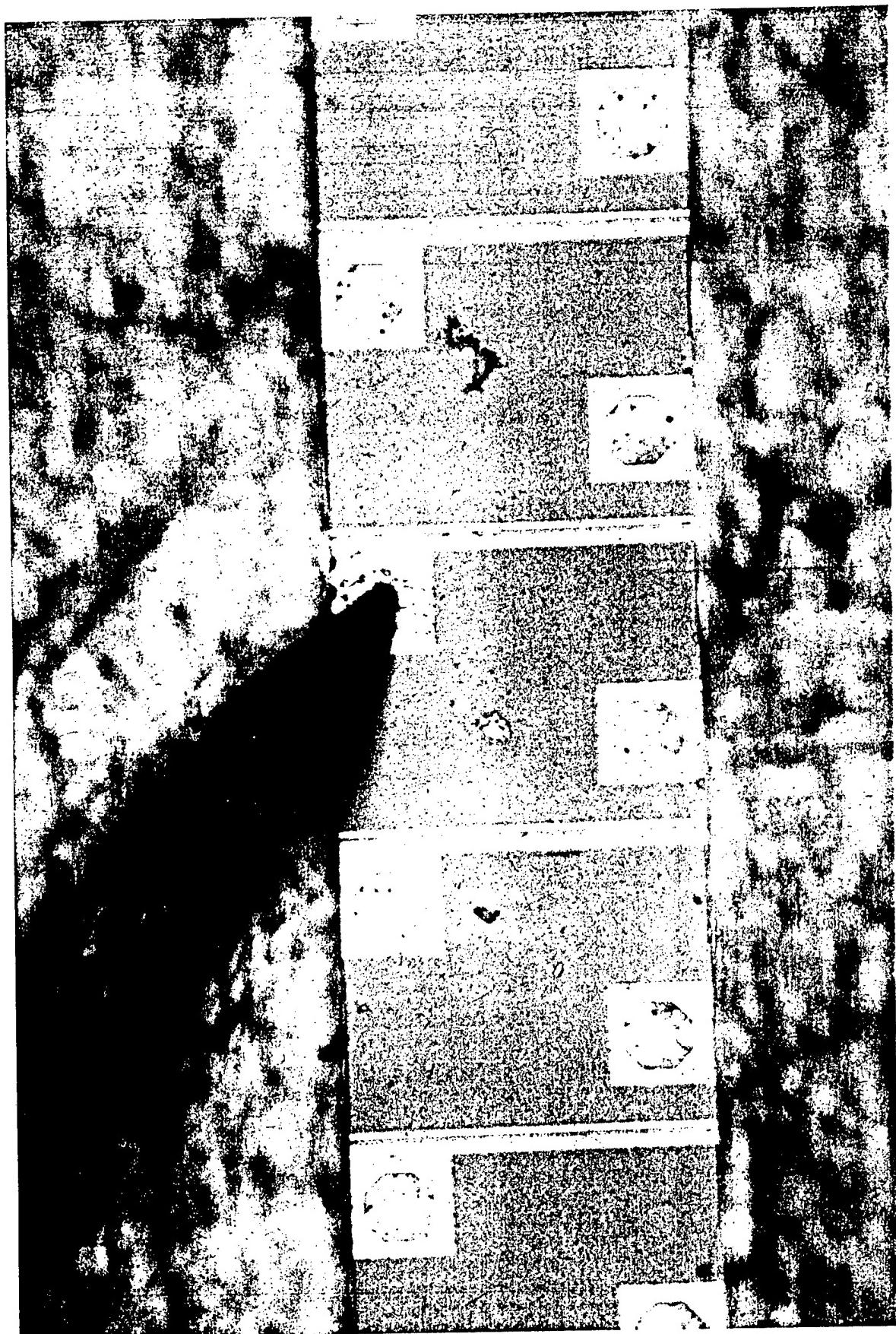
UNC CHARLOTTE

GaAs Laser Array Chip

Laser Diode Arrays

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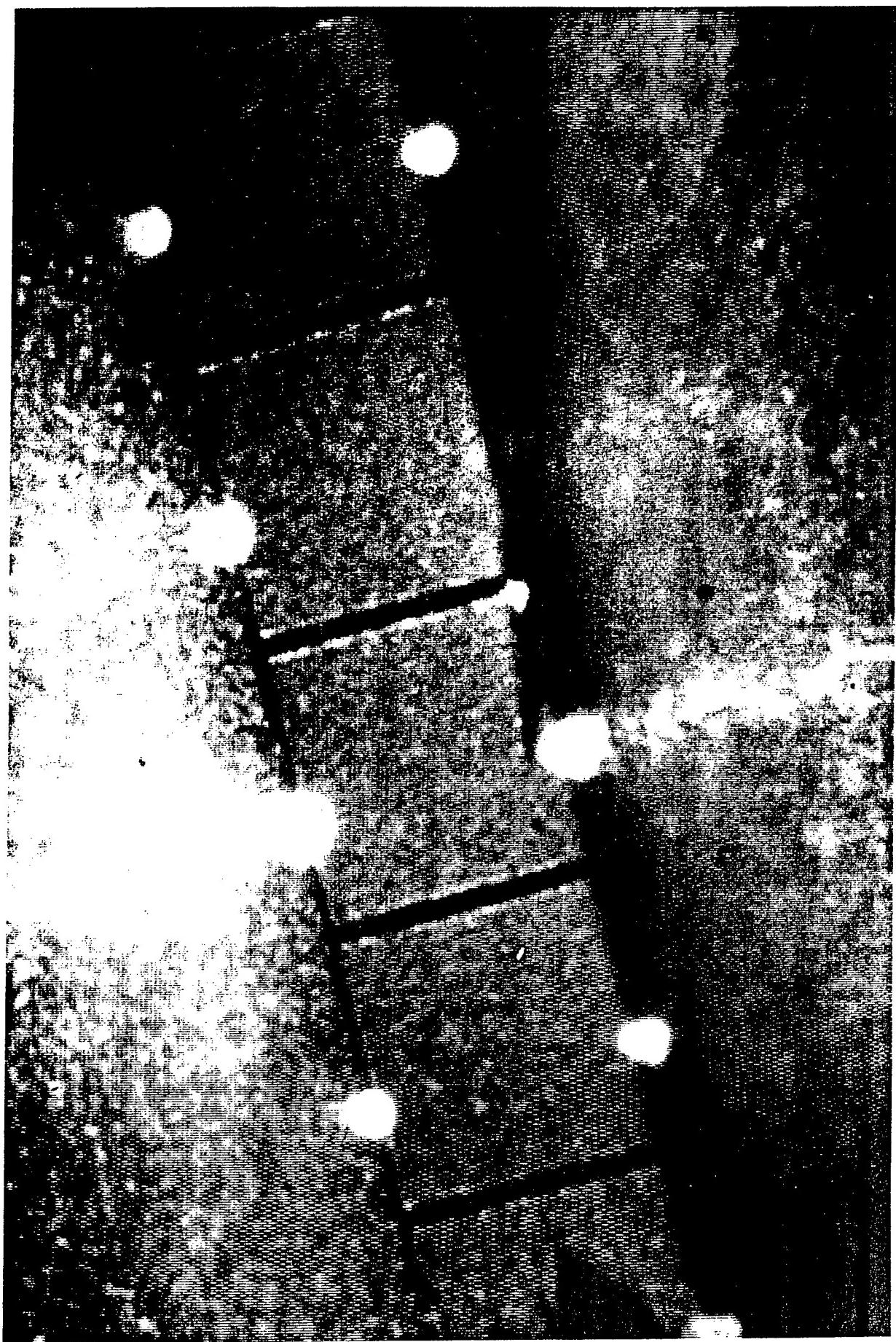
Summary

- Arrays of Edge-emitting Lasers compatible with Flip-chip Bonding Fabricated

- Experimental Measurements:
  - 490 Mbits/sec Operation
  - 4-20 mA Threshold Current

Photodetectors

Issues

- **Integrated Photodetectors**
  - High Connection Density
  - Low Power Consumption

- **High Speed CMOS Detectors**
  - Previous 5Mb/s

- **High Quantum Efficiency**
  - Previous 12%

Improved Photodetector

- Modified MCNC's Standard 1.2 μm CMOS process
- Added 1 additional masking step to create tri-well process
- Detectors located in 8 μm thick low doped intrinsic well
- Increased depletion width from

    ~1 μm to ~6 μm
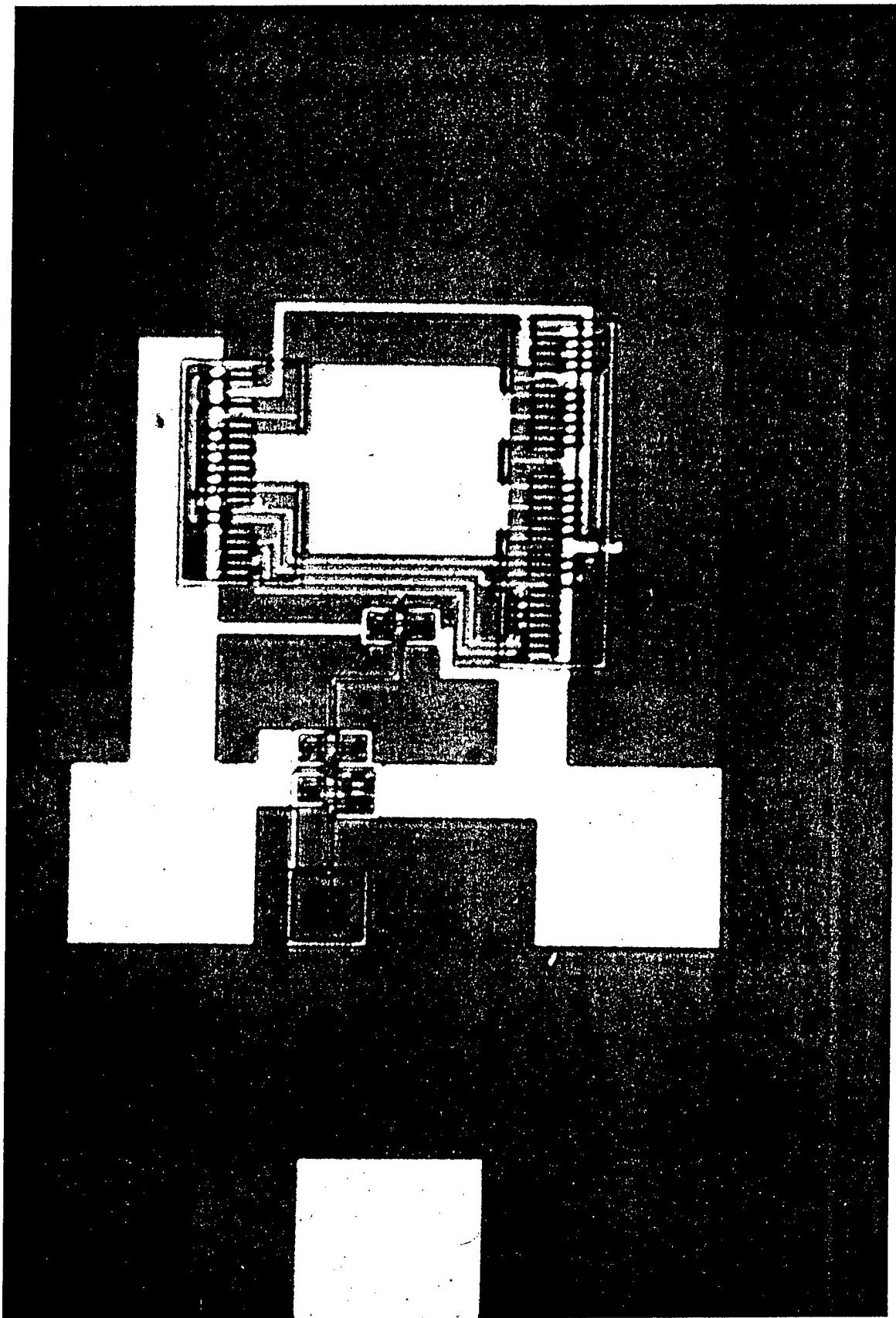
Computer-Generated Holograms (CGHs)

Issues

- High Diffraction Efficiency for Low F# Lasers

- High Diffraction Efficiency for Large Deflection Angles

- Operation over Large Optical Bandwidths ($\sim$10 nm)

- Automated Design (CAD)

Comparison with Previous Experimental CMOS Photo Detectors

	Previous	Improved
Detector Rise Time	34 ns [1]	2.6 ns
Detector Fall Time	36 ns [1]	7.9 ns
Circuit Rise Time	27 ns [2]	4.5 ns
Circuit Fall Time	108 ns [2]	2.0 ns
Modulation Rate	5 Mbits/sec [3]	224 Mbits/sec

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Radially Symmetric Iterative Discrete On-axis (RSIDO) Encoding Method

- Hologram Represented as Set of Concentric Circular Fringes

- Simulated Annealing Used to Find Values of:
    Fringe Widths, Fringe Positions, Phase Values
    (Within Fabrication Constraints)

- Only Change in the Output Pattern Computed on each Iteration

phase transitions

δ

5   6   7

Phase values

$\Delta\rho$
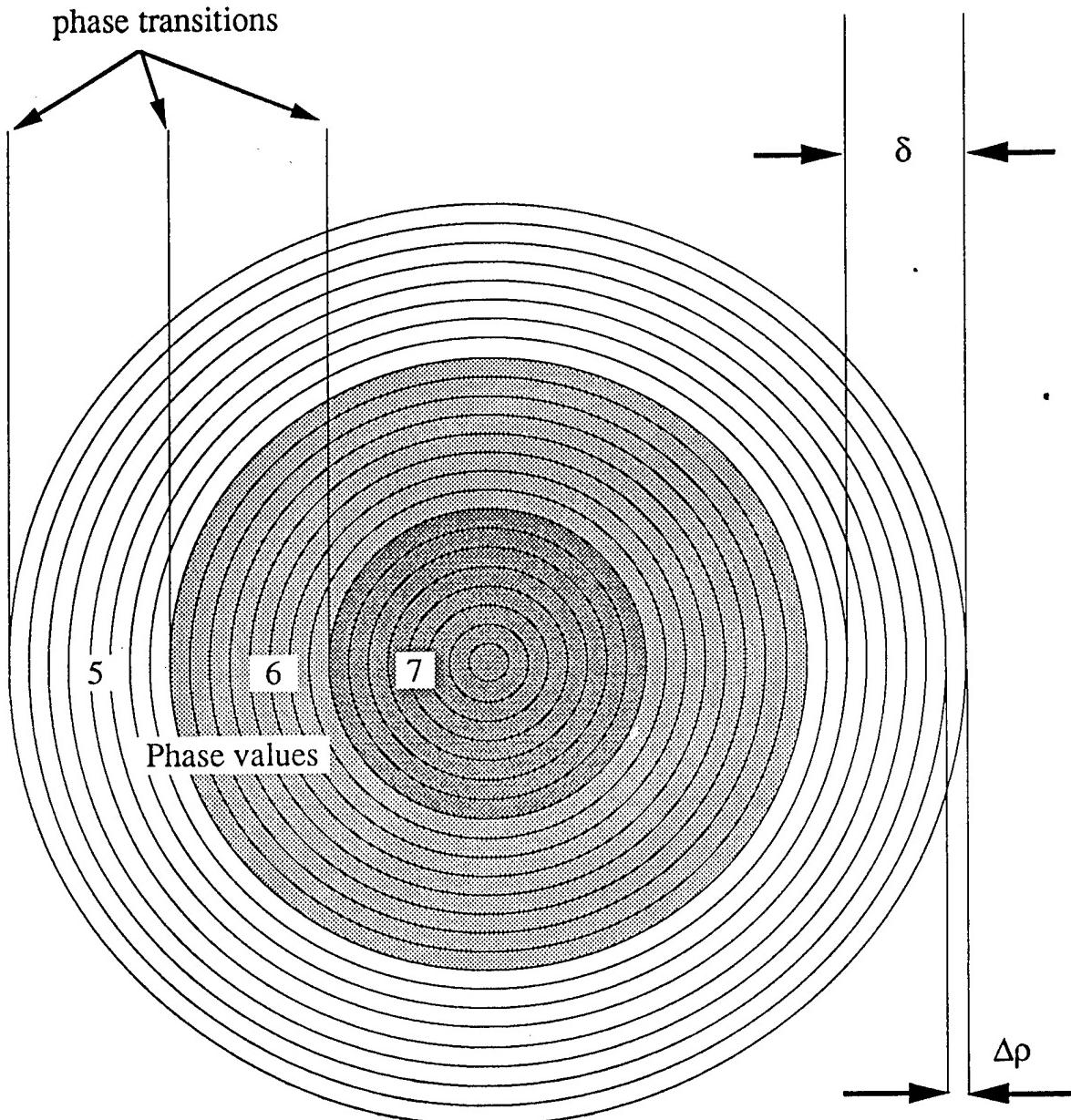
Comparison of RSIDO Design to Analytic Design

Spot Size versus Temperature
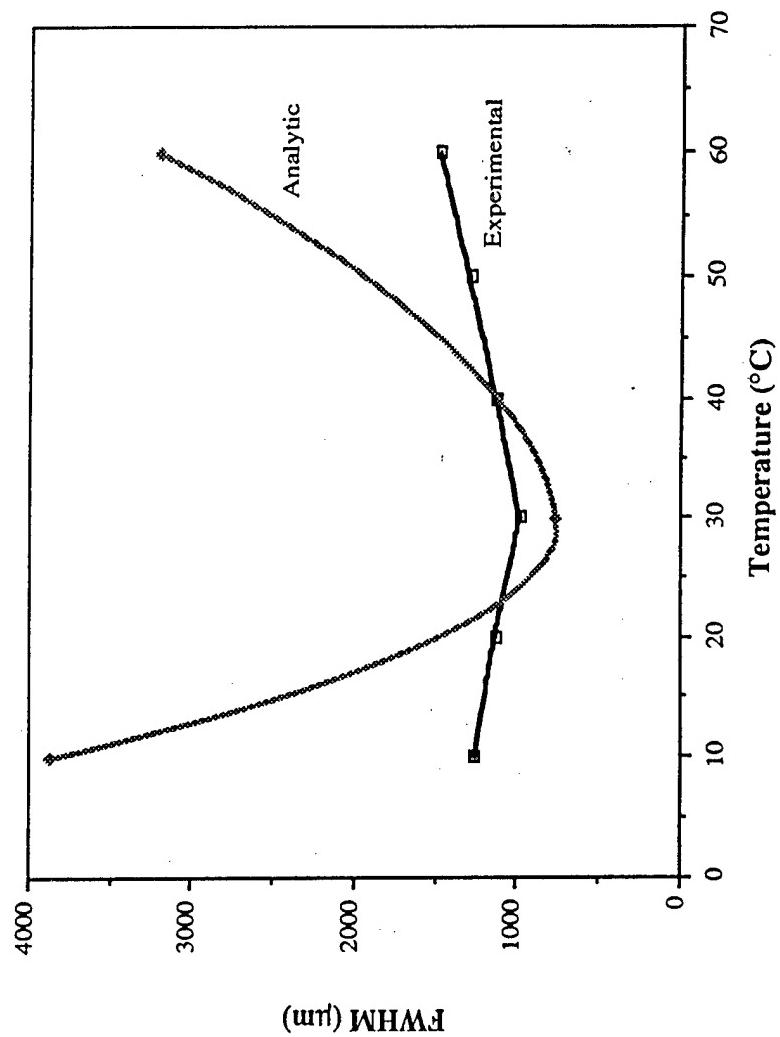
Modified RSIDO for Off-axis Connections

- Hologram is Partitioned into Segmented Annular Rings

- Each Segmented Ring is encoded separately with RSIDO
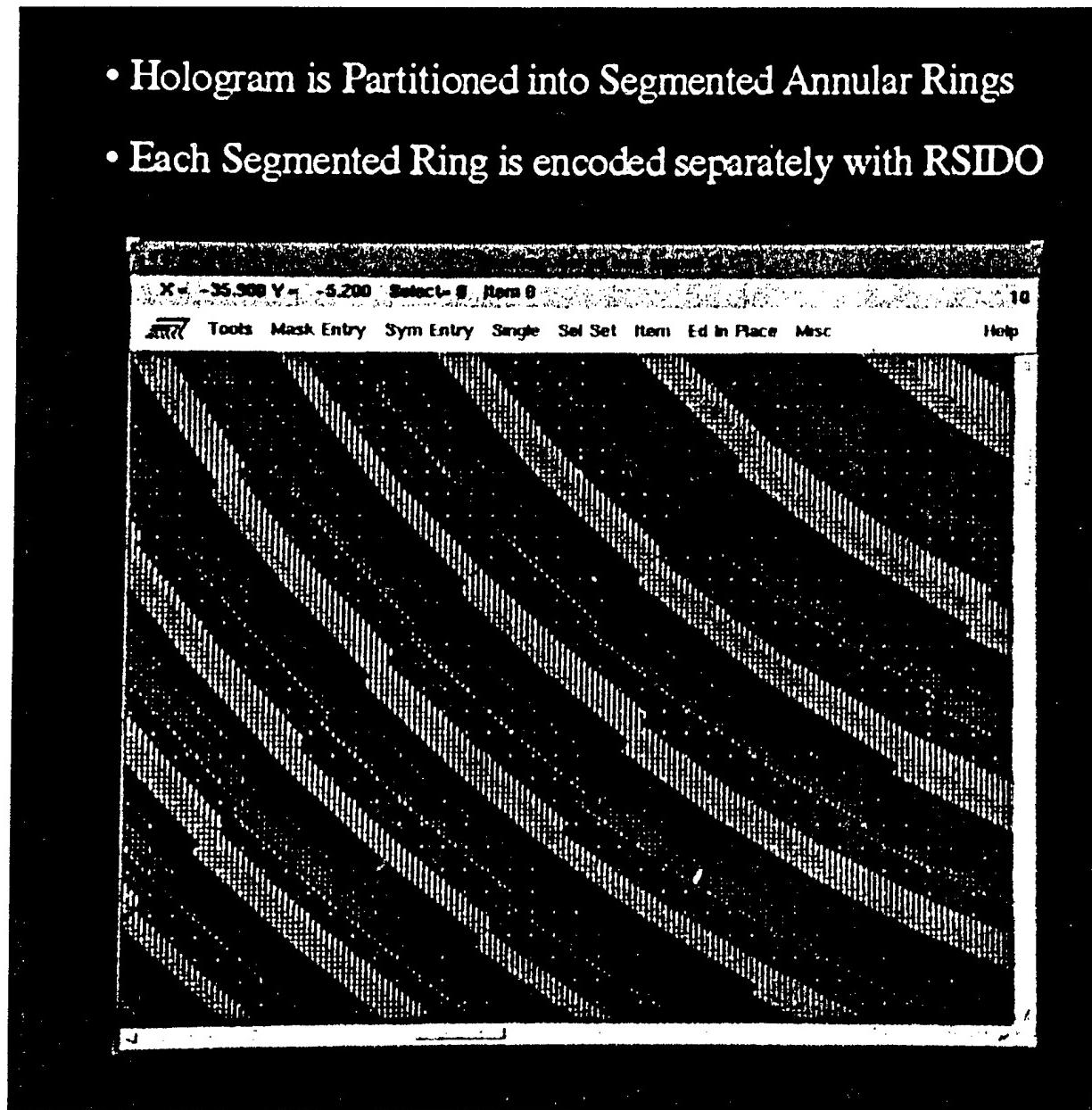
Link Efficiency Summary

Description	DS Efficiency (%)	Fresnel IDO Efficiency (%)	SRP Efficiency (%)
Laser Hologram	37.5	83.6	89.2
Detector Hologram	12.0	37.0	72.3
Link Efficiency	4.5	30.9	64.5

• Tabulated results for a 27° deflection angle and 40mm connection length

Holograms for System 1 Prototype
Summary

- Fanouts ranging from 1 to 3

- Deflection angles ranging from 5 to 27 degrees

- Connection lengths ranging from 5 mm to 8 cm

- 85 total optical links

- Minimum Feature size = 0.5 μm

- Diffraction efficiencies ranging from 50% to 90%,
  Link Efficiencies ranging from 40% to 75%

- Connection Density
  - 1400 I/O's /cm^2
  - Equiv. to electrical thin film MCM with
    - 2.0 μm conductor pitch
    - 2 signal layers
    - 4 inch diameter

Schematic of Optical Interconnect Links
for System 1 Prototype

System Integration

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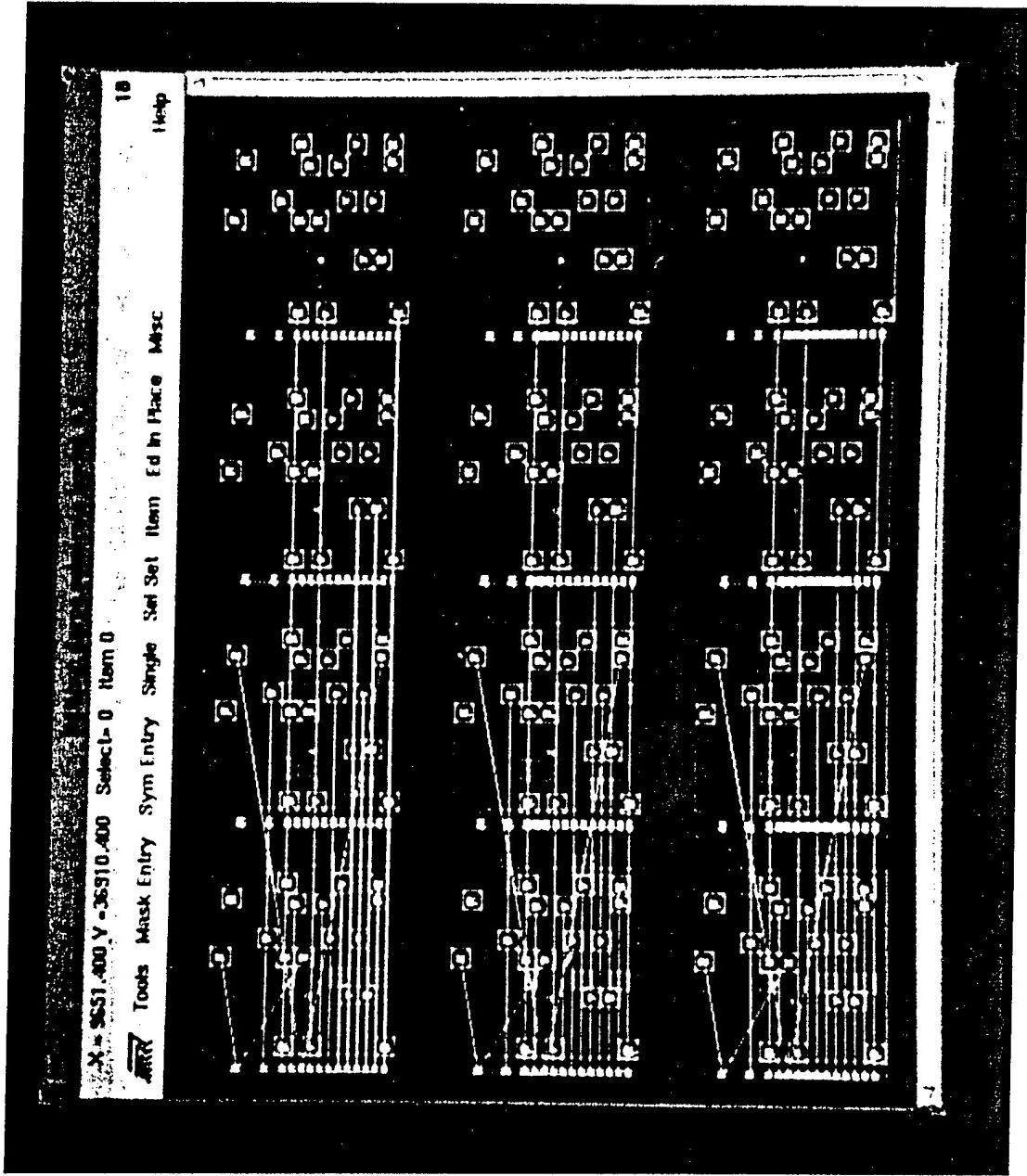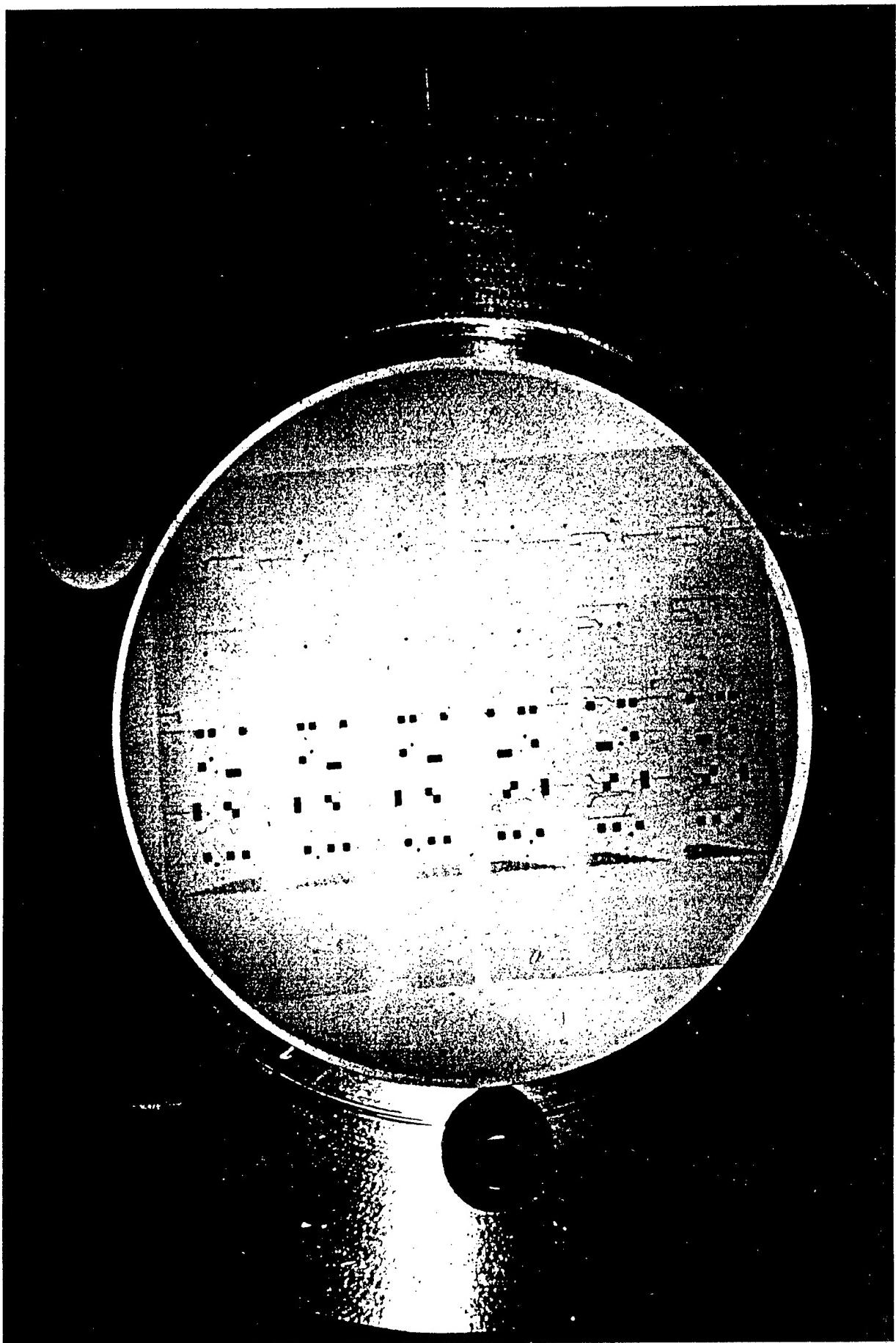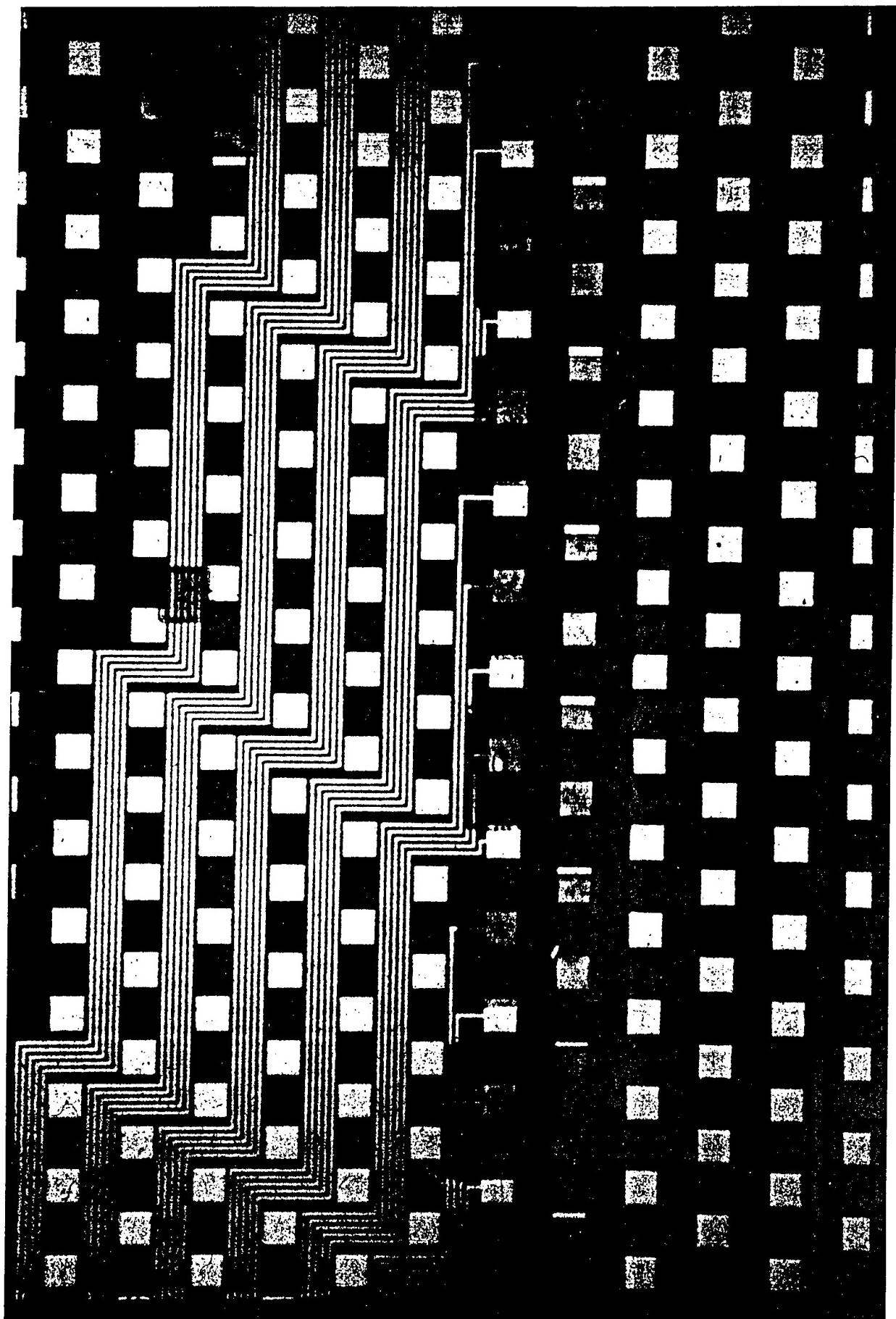
- Alignment
  - **Bonding Components with Required Accuracy**
  - **Aligning CGH to Substrate**
- Redirection of Output of Edge-Emitting Lasers

Alignment Requirements

CGH to Detector : ≈5μm

- Thru-wafer Alignment: 2-3μm

- Flipchip Alignment: 1-2μm
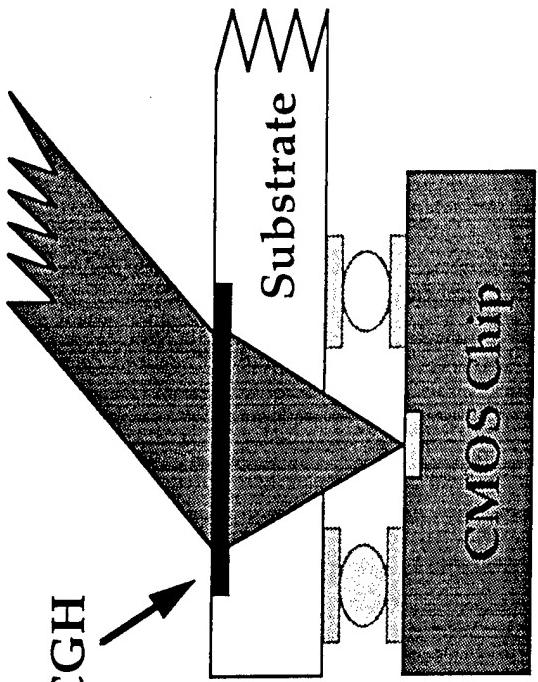
CGH to CGH Alignment: ≈ 100μm

- Most affected by thermal expansion

Scaled Crosssectional View of Laser Chip and Micro-Mirror

Mirror Chip

GaAs Laser Chip

Silicon Chips
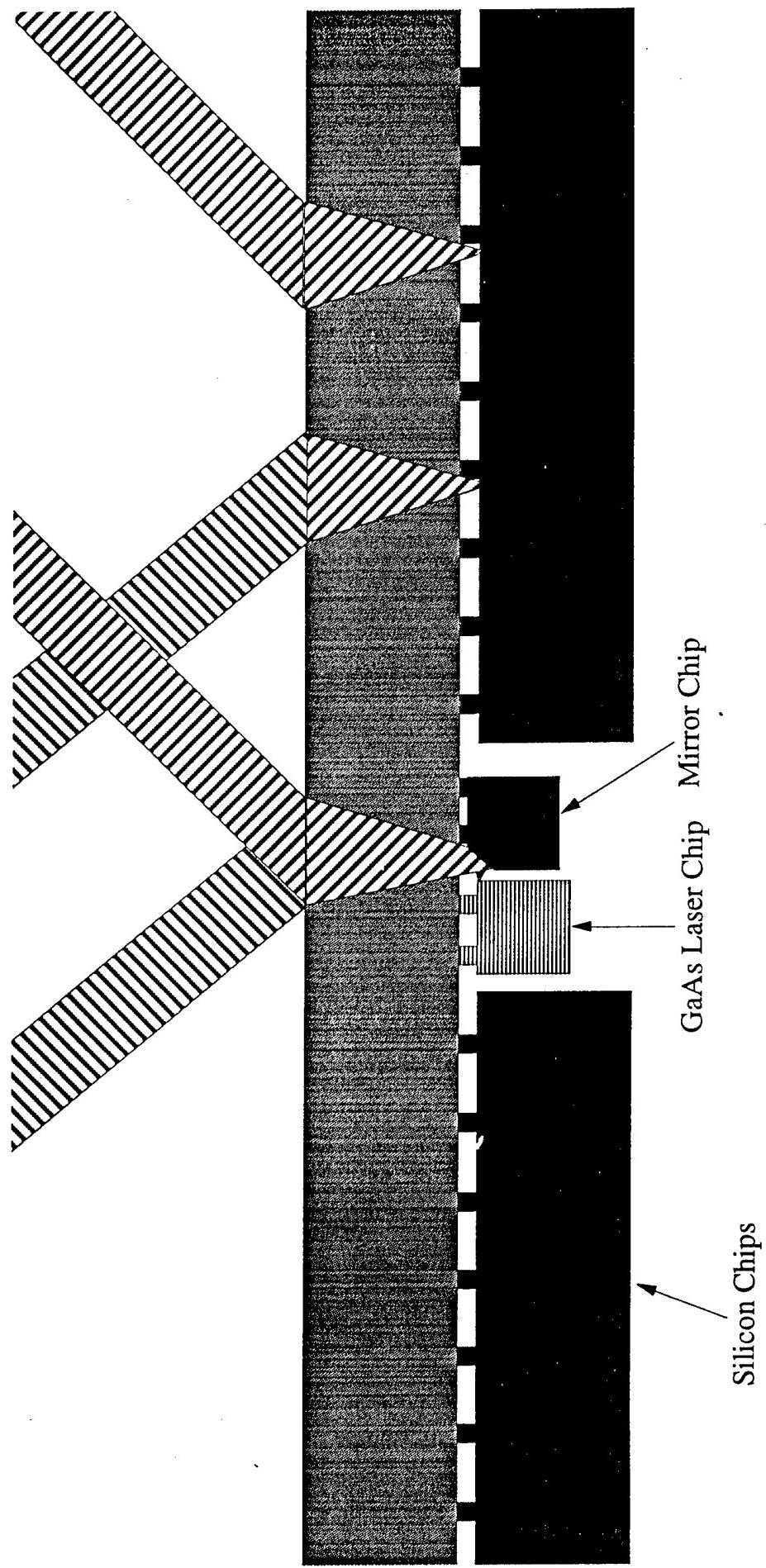
Side View of GaAs Laser Chip and Mirror Chip Bonded to MCM
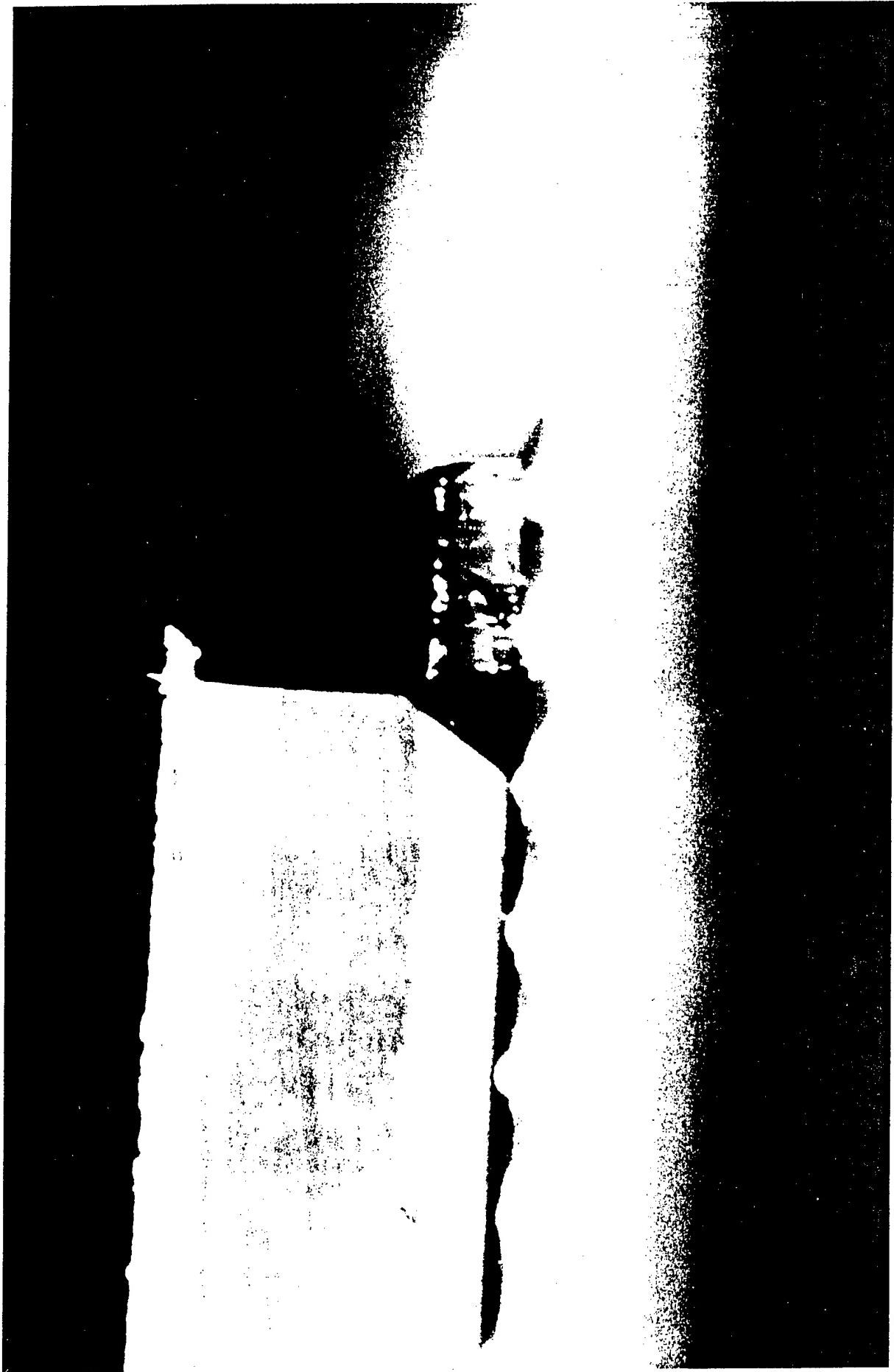
Photograph of portion of System 1 Optically Interconnected MCM
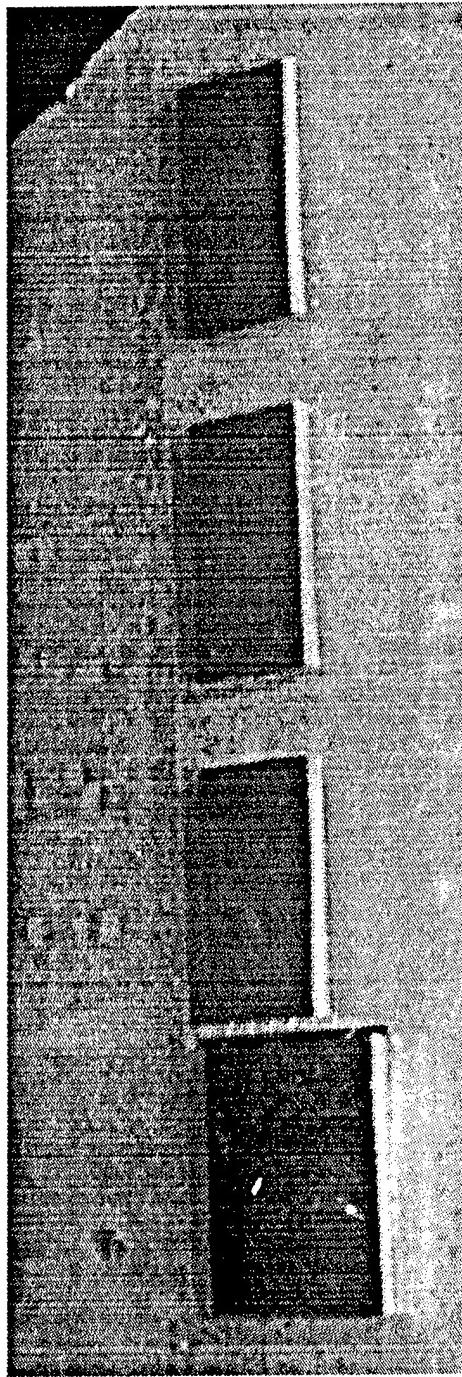
MCM Optical Link Photo

– Detector subhologram
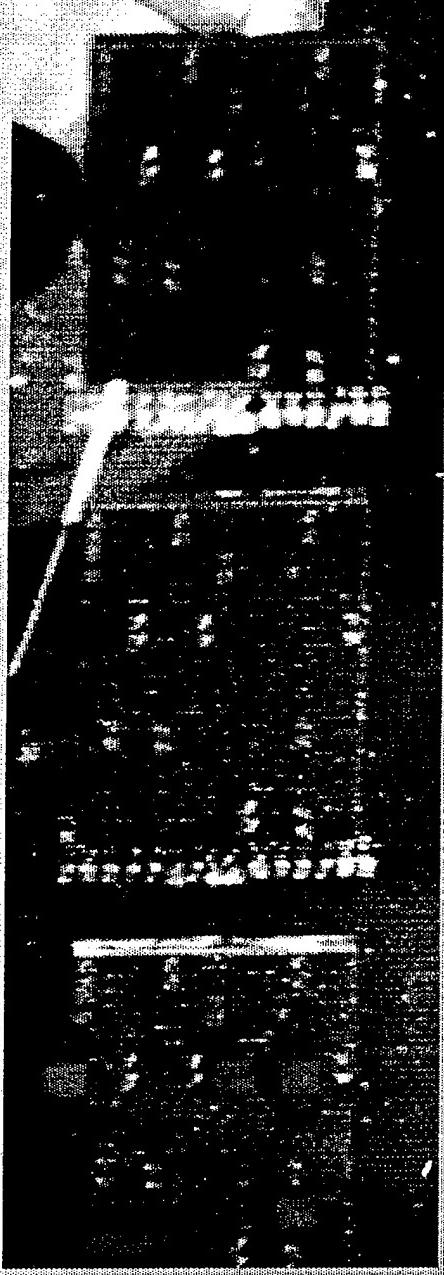
Data=0
(Laser off)

Data=1
(Laser on)

MCM Optical Link Photo
- Receiver Chip

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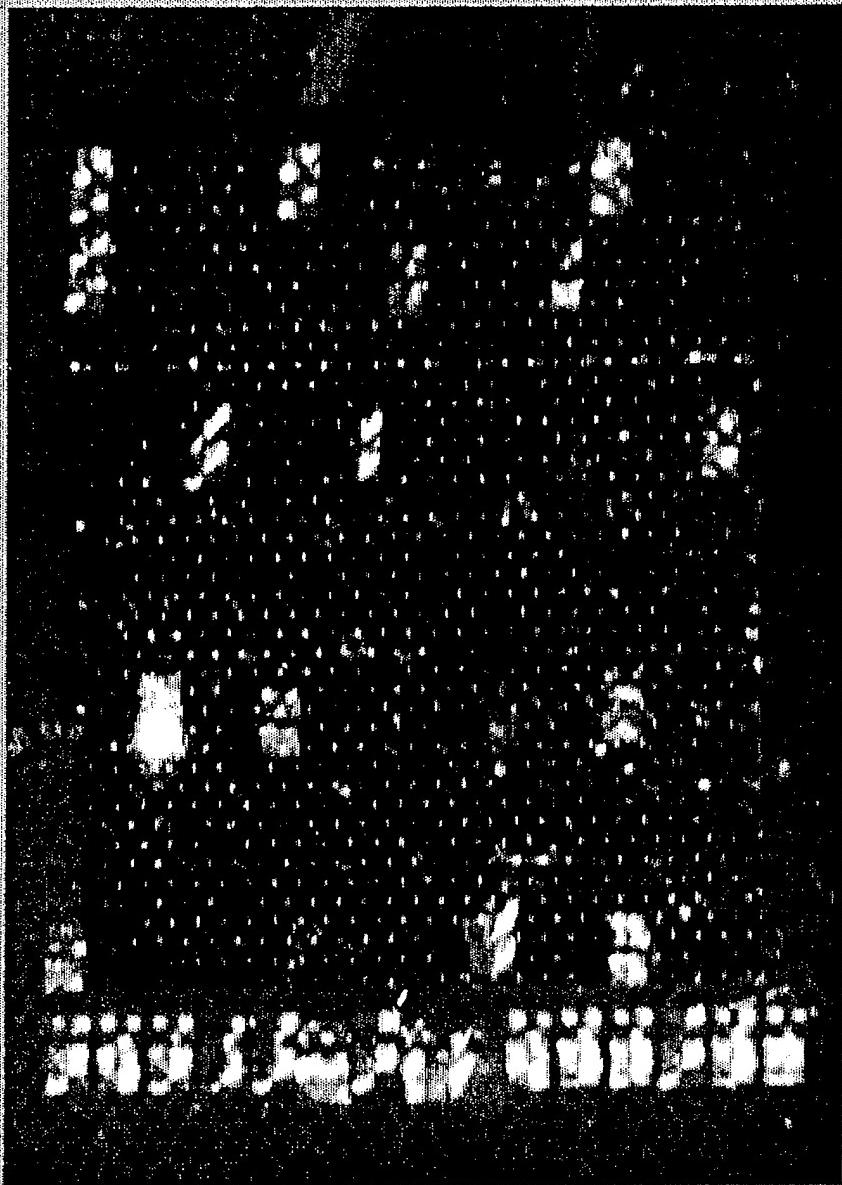
MCM Optical Link Photo

UNCCHARLOTTE
The University of North Carolina at Charlotte
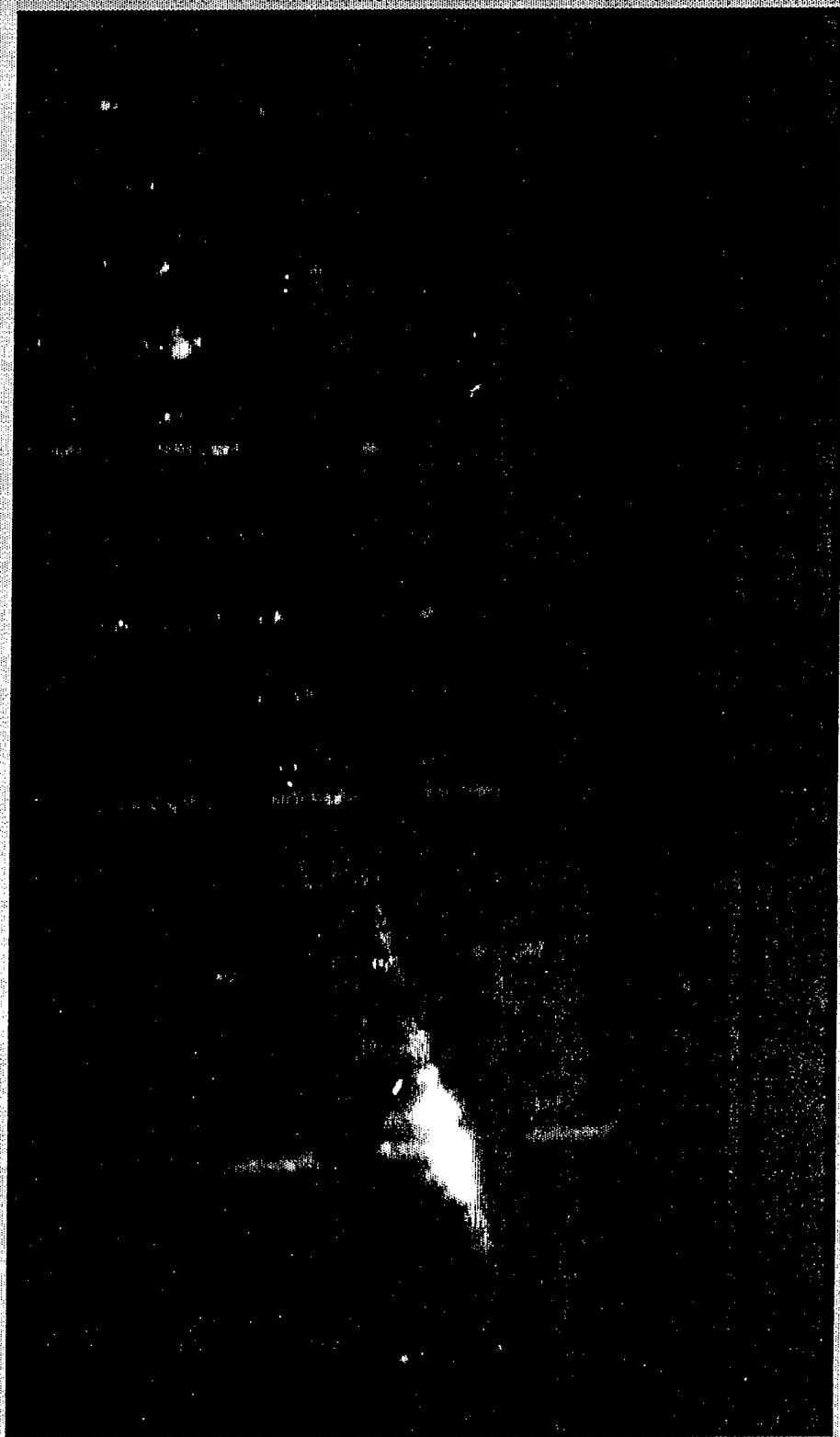
MCM Optical Link Photo

UNCCHARLOTTE
The University of North Carolina at Charlotte
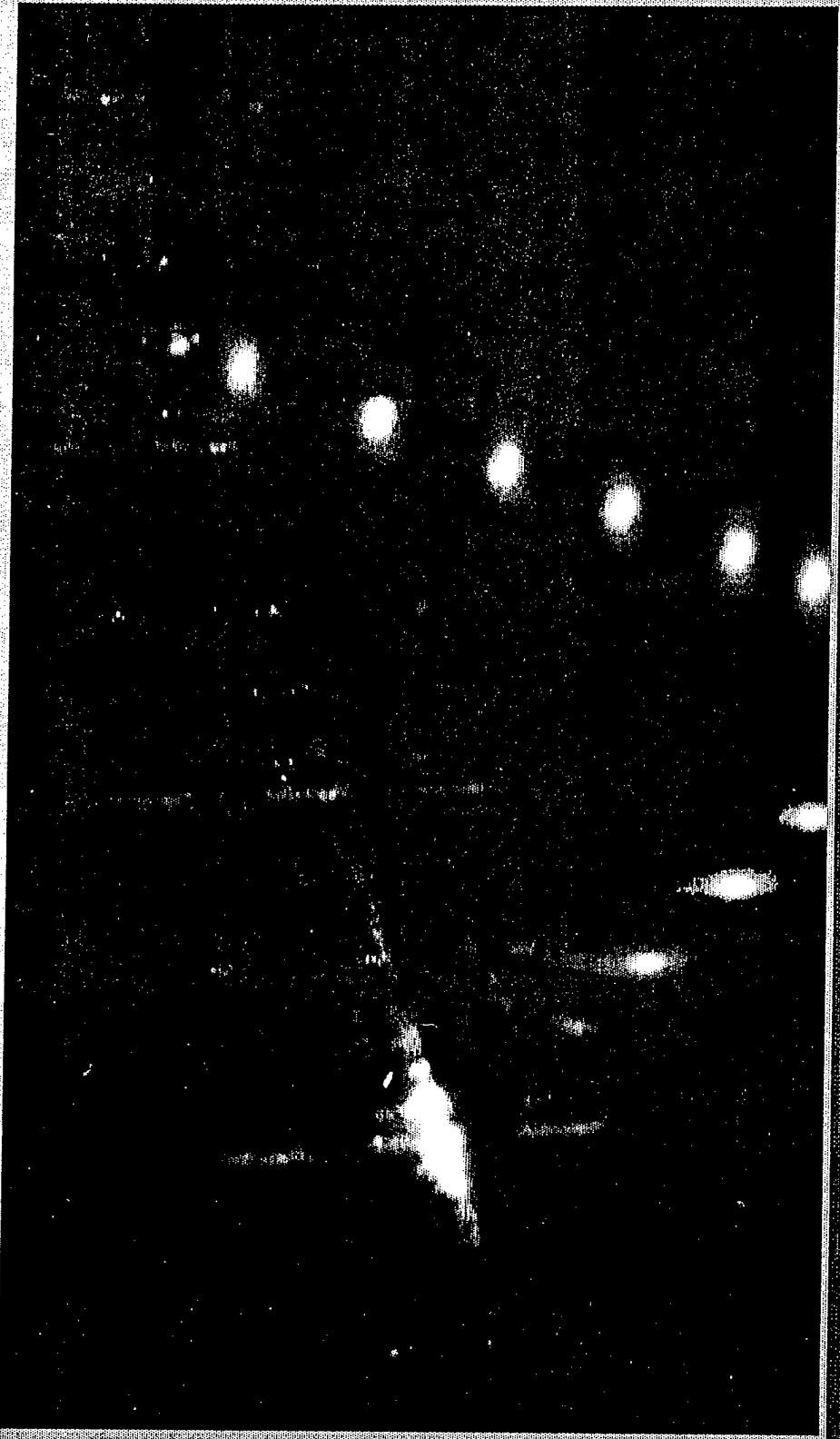
System 1 Prototype Verisons Fabricated

Version	Problems	Achievements
#1	Poor electrical connections to detector & laser chip, No self-alignment	Through-wafer alignment of 1-2 μm
#2	CGH's not operative, residue on substrate	Lasers operative after flip-chip thermal cycling
#3	Test version: No lasers used	Succesful self-aligning flip-chip attatchment of CMOS chips to quarts substrate, ± 1-2 μm accuracy
#4	Through-wafer alignment misalginment: ± 5 μm, Many lasers fail after high-power, DC testing	Demonstration of first complete free-space optical link
#5	Fabrication in process	Fabrication in process

Optical Link Power Budget

Component	Efficiency	Percent Loss	Power after Component (µW)
			3500 Laser Power
Mirror	60%	40%	4860
Misalignment	74%	26%	3429
Fiser CCD	70%	30%	2404
Beam Attenuation	42%	58%	1008
Detector CCD	70%	40%	706
Misalignment	53%	43%	400.0 Detector Power

Optical Link Response Time

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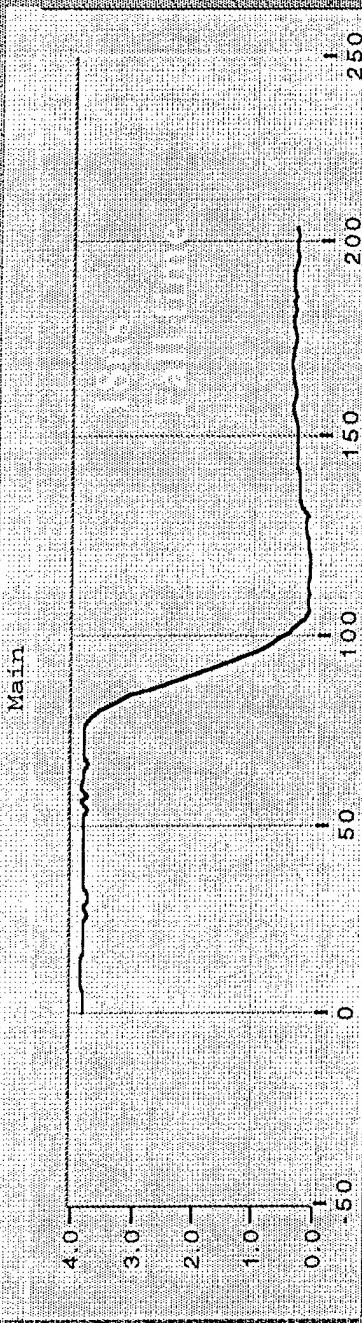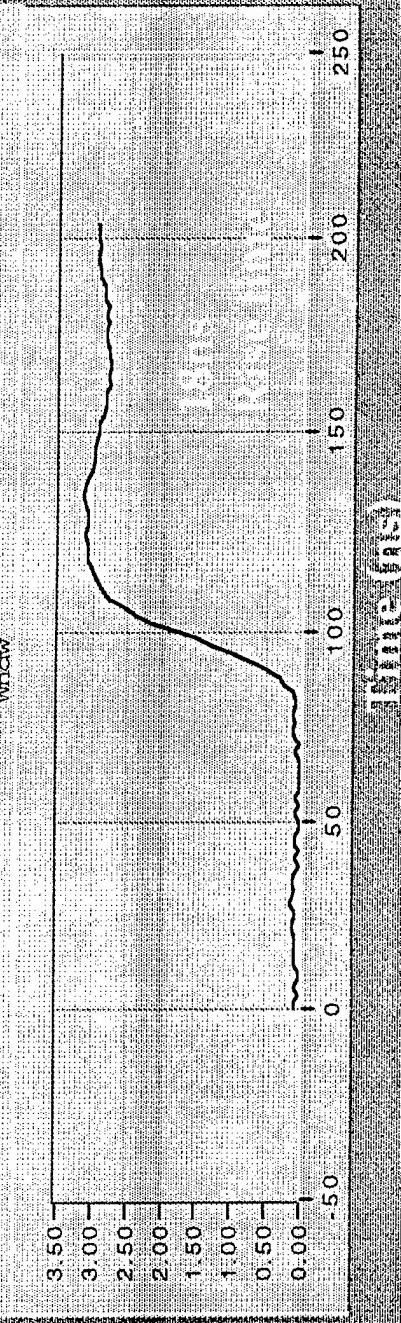
Power Dissipation vs. Data Rate

UNCCHARLOTTE
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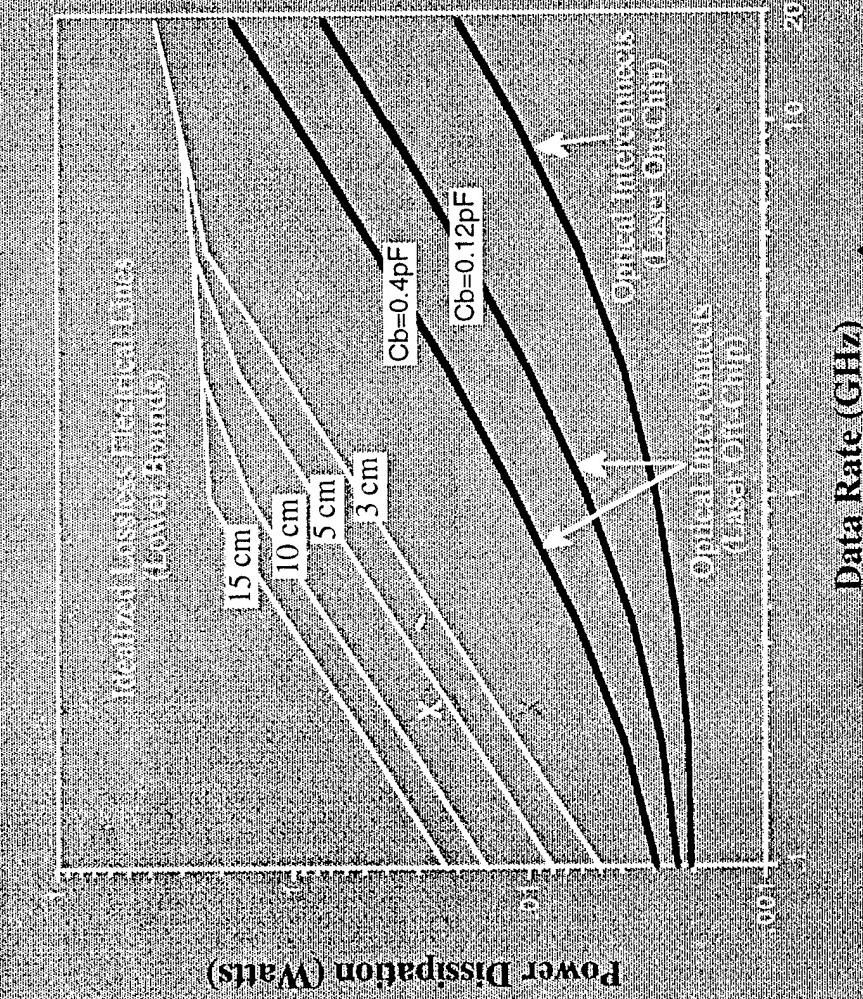
Technology Transfer

- **Hewlett-Packard**
  - Funded several projects at UNC-Charlotte
  - Assembling prototype at HP labs based on technology developed under this program
  - UNC-Charlotte provided substrate with integrated CGHs

- **AMP, Inc**
  - Funded several projects at UNC-Charlotte
  - Successfully transferred holographic fiber optic coupler project
  - Full time AMP engineer relocated to UNC-Charlotte for 1 year

- **Digital Optics Corporation**
  - Start-up small business focussed on diffractive optics, CGHs
  - Commercializing technology, licensed patents developed under this program

- **Others**
  AT&T Bell Labs, MCNC Gigabit Testbed

Conclusions

- Developed Improved Integrated CMOS Detector
    - Increased Datarate of CMOS Compatible Detectors to 220 Mbits/sec (factor of 40 increase)

- New CGH Encoding & Fabrication Techniques
    - Increased Optical Link Efficiency from 4.5% to 64% for 27 degree deflection angle

- Developed Methods for Integrating Lasers, Detectors and CGH's onto the MCM with required Alignment Accuracy

- Demonstrated First Complete Optical Link for an MCM
    - Connection Density Equivalent to conventional fully electronic MCM with:
        - 4 inch diameter
        - 2.0 μm wiring pitch, 2 signal layers

Simplified Free-Space Optical Interconnect
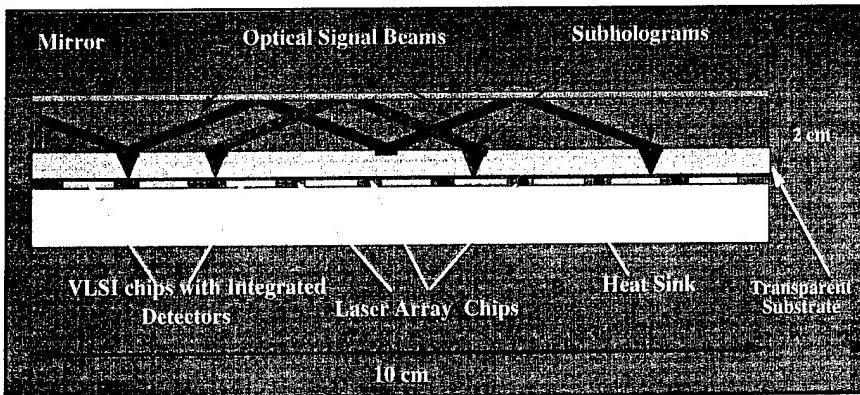
CHARLOTTE, N.C. — Optoelectronic research success may produce an inexpensive way to transfer optical information between electronic devices, a technology that could find widespread use in fiber optic communications and optical computing.

Researchers at the University of North Carolina at Charlotte and the Microelectronic Center of North Carolina in Research Triangle Park have used edge-emitting lasers, holograms and advanced electronic packaging technology in a successful experimental demonstration of a free-space optical interconnect between chips on a multichip module.

Research on optical computing has long focused on two approaches: waveguide interconnects in which laser light is confined to waveguides between chips; and free-space connections in which the light travels through air.

Researchers at the University of North Carolina at Charlotte and the Microelectronic Center of North Carolina have demonstrated this free-space multichip module interconnect.

Near-term drawbacks of waveguides are that while single-level waveguide systems have been demonstrated, more complex devices with multiple crossovers and layers have not, explains UNC Professor Michael Feldman, who led the new research. In the long term, he says, free-space optical interconnects will still have an advantage in connection density.

The problem with free-space interconnects is that previous attempts to demonstrate them have required a large number of components that had to be precisely aligned, requiring the use of many stages and manual "tweaking."

To get around the alignment problem, the North Carolina researchers developed a packaging scheme based on the use of holograms in a double-pass configuration and the use of self-aligning flip-chip technology.

The group fabricated a multichip module based on a planar transparent substrate containing thin-film electrical connections. GaAs laser array chips and silicon VLSI chips with integrated photodetectors were bonded to one side of the substrate, while computer-generated holograms were fabricated on the other side. The laser output was redirected by gold-coated silicon mirrors, and each link was designed to operate at approximately 200 Mb/s.

Feldman's work was funded primarily by a three-year contract from the Advanced Research Projects Agency (ARPA), but the technology is already being transferred to industry through Hewlett-Packard, AMP Inc. and Digital Optics Corp.

The commercial interest comes because free-space optical interconnect technology may lead to a small, fast link between optical fibers and electronic devices, which could drive optical fiber closer to the home. ☐

Stephanie A. Weiss

Electronic Packaging & Production

*Concurrent Engineering for Packaging, Fabrication & Assembly*

MCM Chips Have Free-Space Optical Interconnects

Charlotte, N.C. — The electrical engineering department at the University of North Carolina at Charlotte (UNCC) has produced the first experimental demonstration of free-space optical links between chips on a multichip module (MCM). Scientist Mike Feldman says this prototype optical MCM has a connection density equal to a two-layer, 2.0 µm wiring pitch electronic MCM.

Feldman contends that while guided-wave MCM optical interconnects have been demonstrated in the past, they do not have nearly the connection capacity of free-space links, as demonstrated by this prototype.

"In fact," declares Feldman, "the guided-wave optical interconnect MCM links that have been demonstrated have all been only single-level systems that severely limit the connection capacity for many interconnection networks. In the past, in part due to the lack of a good free-space interconnect prototype demonstration, many researchers have claimed that guided-wave interconnects are more viable and more near-term than free-space interconnects. However, we believe that our prototype demonstration will convince many that free-space interconnects may be the most viable means of achieving very high-density connections."

Optically Interconnected MCM

Mirror   Optical signal beams   Subholograms

2.0 cm

VLSI chips with integrated detectors   Laser array chips   Transparent substrate   Heat sink

10.0 cm

Cross-section of an optically interconnected multichip module.

The UNCC optically interconnected multichip module (OIMCM) design is based upon flip chip and computer generated hologram (CGH) technologies. The circuit contains 85 optical links, three GaAs laser array chips and 12 silicon CMOS detector chips. Each laser array chip contains 32 edge-emitting lasers. The output of the lasers is redirected by the use of a gold-coated silicon micro-mirror. The links are routed through a transparent substrate and are designed to operate at about 200 Mbit/second.

Feldman credits three major technological improvements that have provided increased impetus for free-space optical interconnects: 1) high-speed photodetectors integrated within CMOS VLSI chips, 2) new CGH designs allowing higher diffraction efficiency at large deflection angles, and 3) advanced flip chip bonding techniques for achieving the required alignment accuracies.

Mike Feldman can be reached at 704-547-2302.

ELECTRONICS PACKAGING

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